Remarks

Claims 1-15 are pending in the application. Applicant respectfully asks Examiner to please add Claims 16-18. Claims 1, 2, 7, 10-12, 14 and 15 have been amended. Claims 1-6, 8, 9, 12 and 13 have been rejected under 35 U.S.C. § 102(b). Claims 7, 10, 11, 14 and 15 have been rejected under 35 U.S.C. § 103(a). In view of the following remarks, reconsideration and withdrawal of these grounds for rejection is requested.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-6, 8, 9, 12 and 13 stand rejected under 35 U.S.C. § 102 (b) as being anticipated by Japanese Patent JP58-181310 ("Sakaguchi").

The Office Action states that Sakaguchi discloses all of the elements of Claims 1 and 12 of the current application. Claims 1, 2 and 12 have been amended.

Claim 1 now reads:

> A switch circuit comprising: a first differential amplifier pair providing a portion of an isolation channel; a second differential pair providing a portion of a transmit channel; and a third differential amplifier pair providing a control bias for selecting either the transmit channel or the isolation channel, wherein the control bias maintains a substantially constant current density. **[Emphasis Added]**.

Therefore, the third differential amplifier pair provides a control bias that maintains a substantially constant current density for selecting either a transmit or an isolation channel. The substantially constant current density prevents current depletion in the control bias, thus ensuring extremely high-speed switching between the two channels. (Paragraph 0018).

On the other hand, Sakaguchi discloses a "conventional" voltage gain control amplifier. (Figure 1). The gain varies depending on the value of the voltages applied to the first and second

voltage control terminals, V_1 and V_2. The gain variations cause fluctuations in the output DC potential. Sakaguchi further discloses an improvement on the voltage gain amplifier of Figure 1. The improved circuit is designed so that the output DC potential does not fluctuate in cases where the gain is variable depending on the values of the control voltages V_1 and V_2. (See Figure 3).

In sharp contrast to the Applicant's claims, Sakaguchi does not contemplate high speed switching, switching between an isolation channel and a transmit channel, or the challenge of isolating an input signal in high circuit density environments, such as on an integrated circuit. Enclosed for the Examiner's convenience is an English translation of Sakaguchi. The circuit shown in Figure 1 discloses a control bias wherein the emitters of the transistors (1) and (2) are connected to each other via resistors (5) and (6), which are connected in series, and a current source (7) which is connected between the connection point and the ground point of resistor (5) and resistor (6). The resistors (5) and (6) will impede the circuit from maintaining a constant current density in the control bias. As such, it is respectfully submitted that the circuit configuration in Figure 1 cannot perform high-speed switching between an isolation channel and a transmit channel for applications such as, for example, pulsed radar systems. Therefore, Figure 1 cannot anticipate Claim 1. Withdrawal of the rejection with respect to Claims 2-6, 8, 12 and 13 is also requested.

Claim 9 discloses at least one inductor coupled to each of the respective collectors of the at least two transistors of the second differential amplifier pair. Sakaguchi discloses that only the collector of transistor (11) is connected to the power supply terminal (12) via resistor (13). The collectors of transistors (8), (9) and (10) are all connected directly to the power supply terminal

(12). (Figure 1). This is not the Applicant's circuit. Therefore, Sakaguchi cannot anticipate Claim 9. Withdrawal of the rejection with respect to Claim 9 is therefore requested.

Claim Rejections Under 35 U.S.C. § 103

Claims 7, 10, 11, 14 and 15 stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over Sakaguchi.

The Office Action states that Sakaguchi discloses all of the limitations of Claim 7 except for that the circuit is formed as an integrated circuit on a Silicon germanium substrate. Claim 7 has been amended. Further, Claim 7 is dependent on Claim 1. For the reasons discussed above, Claim 1 is not anticipated or rendered obvious by Sakaguchi. Therefore, the limitations of Claim 7 cannot be obvious in light of Sakaguchi. Withdrawal of the rejection is requested.

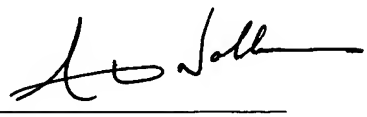
With regard to Claims 10, 11, 14 and 15, the Office Action states that Sakaguchi discloses all of the limitations of the claims except for that the pulse width of the control bias is less than 500 picoseconds and/or between 200-300 picoseconds.

Claims 10, 11, 14 and 15 have been amended. Claims 10 and 11 depend on Claim 1 and Claims 14 and 15 depend on Claim 13, which is dependent on Claim 12. For the reasons cited above, Sakaguchi does not anticipate or render obvious Claims 1 and 12. Therefore, Claims 10, 11, 14 and 15 are not rendered obvious in light of Sakaguchi. In addition, Sakaguchi does not suggest or disclose a substantially constant current density that is sufficient to enable a pulse width of a control voltage to be less than 500 picoseconds and/or between 200-300 picoseconds. Withdrawal of the rejection is requested.

Conclusion

In view of the foregoing remarks, Applicants submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

Respectfully submitted,



Paul A. Taufer
Reg. No. 35,703
Andrew A. Noble
Reg. No. 48,651

AAN:pam
(215) 656-3303